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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/652,653	08/28/2003	Atsushi Tanaka	16869S-092100US	1913
20350	7590	07/07/2005	EXAMINER	
TOWNSEND AND TOWNSEND AND CREW, LLP TWO EMBARCADERO CENTER EIGHTH FLOOR SAN FRANCISCO, CA 94111-3834			NGUYEN, VIET Q	
		ART UNIT	PAPER NUMBER	2827

DATE MAILED: 07/07/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/652,653	TANAKA ET AL.	
	Examiner	Art Unit	
	Viet Q. Nguyen	2827	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) Responsive to communication(s) filed on Election filed on 5/20/2005.
- 2a) This action is FINAL. 2b) This action is non-final.
- 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) Claim(s) 1-11 is/are pending in the application.
- 4a) Of the above claim(s) 11 is/are withdrawn from consideration.
- 5) Claim(s) _____ is/are allowed.
- 6) Claim(s) 1 and 2 is/are rejected.
- 7) Claim(s) 3-10 is/are objected to.
- 8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) The specification is objected to by the Examiner.
- 10) The drawing(s) filed on _____ is/are: a) accepted or b) objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) All b) Some * c) None of:
 1. Certified copies of the priority documents have been received.
 2. Certified copies of the priority documents have been received in Application No. _____.
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|---|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____. |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date <u>12/04/09/03/08/28/</u> | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| | 6) <input type="checkbox"/> Other: _____. |

DETAILED ACTION

1. The applicants' election of Group 1, claims **1-10** on **5/20/2005** is acknowledged.
Claims **1-10** are present for examination.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims **1-2** are rejected under 35 U.S.C. 102(b) as being anticipated by **Byers et al (5,809,543)**.

Regarding claim 1, **Byers et al (see Fig.1)** clearly shows an overall network storage control system (SAN/NAS) that includes a plurality of disks (mains storage units 16s) for storing data, a plurality of storage controllers (SC1 to SC4), interfaced with respective host computers, for receiving their respective I/O commands and thus for trolling the storage disks (MSU 16) in accordance with such respective I/O commands. For example, col. 11 describes the interaction between instruction processors (IPs 12) and the storage controller (SC4) from controlling writing/reading data to/from the memory units. Note that Fig.1 also shows that all these storage controllers (SC1 to SC4) are interconnected through the network cables (20, 22, 28, 30, 26, etc.) that altogether making up a

"network" for interconnecting all these controllers together as claimed.

Furthermore, Fig. 2 shows that one of the controller (i.e., IOC 32 of controller SC3, SC4) can have a plurality of block interfaces to the host computer (IP) if desired; that is data can be moved in **blocks** from the respective storage disks (or peripheral systems) to/from the host computers (i.e., IPs 12) through the remote adapter (36) and through these storage controllers therebetween. Also, Fig. 4 shows that the storage controller can have a "**file**" interface (i.e., see file structures 106s & 108s) to the cache storage (see also Fig. 2, cache disk controller) as well-known in the art (Fig. 2)

Regarding claim 2, channel adapter is shown in Fig. 2, and disk adapter is shown in Fig. 3 (cache disk controller).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

5. Claims 1-2 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Davis et al (US 2002/0087720 A1)**.

Davis et al (see Fig. 2) clearly shows an overall storage control system (SAN/NAS) that includes a plurality of disks (330) for storing data, a plurality of **interconnected** storage controllers (see IO controllers in inside the plurality of IO

units 310), with each such IO unit interconnected to each other through the fabric switch (300) and also interfaced with the plurality of respective host computers (i.e., host processors 10 & 20) through same fabric switch 300. Paragraphs [0018] to [0019] further mention the interface between host computers and the controllers for accessing to memory disks by using I/O commands from the processors. Note that Fig. 2 also shows that all these storage controllers are interconnected through the fabric switch (300) that altogether making up a "network" for interconnecting all these controllers together as claimed.

Regarding the claimed "block interface" not clearly spelled out in this reference, it is noted that Fig. 1 (see also Para [0019]) did mention that a "direct memory access (**DMA**)" can be carried out remotely between the any processor and the controllers. However, since the concept of "DMA" is already well-known to one skilled in this art as a means for synchronously transferring data "blocks" between any two communicating hosts, i.e., controllers or CPUs, thus obviously suggest that any memory or disk controllers of Davis et al also have a similar "block interface" as an interface to any host computer as well.

Regarding the claimed "file interface" not clearly spelled out in this reference, it is noted that Fig. 2(se also Para [0022]) discuss the us of software program/codes to access larger file system using OS services, application layers, and/or programming languages (i.e., C++) for accessing to/from the memory/disk adapters. Thus, in so far as the memory block and/or chunks of data only appear to any computer user as "file", these application/OS software layers obviously

acting equivalently as the claimed “file interface” between these storage/disk controllers and the host processors (10,20) for performing the job of memory accessing if any.

Regarding claim 2, “channel/disk adapters” are clearly shown in Fig. 2 (i.e., see host channel adapter 60, IO device interface 320, and disks 330) for interfacing with low-level IO devices.

6. Claims 1-2 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Weber (US 2003/0225735)**.

Weber (see Fig. 1) clearly shows an overall storage control system (SAN/NAS) that includes a plurality of disks (130) for storing data, a plurality of **interconnected** storage controllers (see controller elements in inside the plurality of storage elements 122, 124), with each such element/controller unit also interconnected to each other through the fabric switch (120), and each unit also interfaced with the plurality of respective host computers (i.e., host processors 132 to 136) through same fabric switch 300 and the I/O modules 1 to N).

Paragraphs [0017] to [0034] discusses in detail the structure, operation, and the interface between host computers and these controller elements for accessing to memory disks (130) by using I/O commands from the processors. Note that Fig. 2 also shows that all these storage controllers are interconnected through the fabric switch (120) that altogether making up a “network” for interconnecting all these controllers together as claimed.

Regarding the claimed “block interface” not clearly spelled out in this reference, it is noted that Fig. 1 (see also Para [0018]) did mention that a “direct memory access (*DMA*)” can be carried out between the any processor and the controllers using the remote DMA protocol. However, since the concept of “DMA” is already well-known to one skilled in this art as a means for synchronously transferring data “blocks” between any two communicating hosts, i.e., controllers or CPUs, thus obviously suggest that any memory or disk controllers of Davis et al also have a similar “block interface” as an interface to any host computer as well. Furthermore, Para [0029] mentions that data can be stored into a particular storage device using “object” or “file” concept.

Regarding the claimed “file interface” not clearly spelled out in this reference, it is noted that Fig. 1 shows the use of an “object “converting element (142) for converting the block of data to/from a file object to be stored or accessed to the storage disks, if necessary, thus obviously suggest that these converting elements act equivalently as the claimed “file interface” as recited.

Regarding claim 2, “channel/disk adapters” are clearly shown in Fig. 2 (i.e., see host channel adapter 60, IO device interface 320, and disks 330) for interfacing with low-level IO devices.

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7. Other claims are **objected** (as being dependent upon claim 1), but contain **allowable subject matter (not shown or suggested over prior arts of record)** for the following reasons:

- Claims 3, 5-10 recites the “file server unit”, “failure information”, and its communication structure, etc., which is not shown or fairly suggested elsewhere in the prior arts;
- Claim 4 recites the use of a shared “control memory” between plurality of controllers;

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Viet Q. Nguyen whose telephone number is (571) 272-1788. The examiner can normally be reached on 7am-6pm (EST).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Hoai Ho can be reached on (571) 272-1777. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Viet Q Nguyen
Primary Examiner
Art Unit 2827

VN
V. Nguyen
7/2/2005

V. Nguyen